**IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

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|---|---|
| ACORN SEMI, LLC,<br>*Plaintiff,*<br><br>v.<br><br>SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR, LLC,<br>*Defendants.* | Civil Action No. 2:19-cv-00347-JRG |

**CLAIM CONSTRUCTION MEMORANDUM OPINION AND ORDER**

Before the Court is the opening claim construction brief of Plaintiff Acorn Semi, LLC ("Plaintiff") (Dkt. No. 65, filed on August 21, 2010),[1] the response of Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, LLC (collectively, the "Defendants") (Dkt. No. 69, filed on September 4, 2020), and Plaintiff's reply (Dkt. No. 71, filed on September 11, 2020). The Court held a hearing on the issues of claim construction and claim definiteness on October 5, 2020. Having considered the arguments and evidence presented by the parties at the hearing and in their briefing, the Court issues this Order.

[1] Citations to the parties' filings are to the filing's number in the docket (Dkt. No.) and pin cites are to the page numbers of the documents.

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## I. BACKGROUND

Plaintiff alleges infringement of six U.S. Patents: No. 7,084,423 (the "'423 Patent"), No. 8,766,336 (the "'336 Patent"), No. 9,209,261 (the "'261 Patent"), No. 9,461,167 (the "'167 Patent"), No. 9,905,691 (the "'691 Patent"), and No. 10,090,395 (the "'395 Patent") (collectively, the "Asserted Patents"). Each of the Asserted Patents is entitled Method for Depinning the Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions. The patents are related and each claim priority to the application that issued as the '423 Patent, which was filed on August 12, 2002.[2]

In general, the Asserted Patents are directed to technology for improving the performance of conductor/semiconductor junctions by separating the conductor (such as a metal) from the semiconductor with an interface layer to address surface state effects on the Schottky barrier. The appropriate interface layer can serve to depin the Fermi level of the semiconductor to enable tuning of the height of the Schottky barrier of the junction. Depinning may involve (1) passivating the semiconductor by terminating dangling bonds on the surface of the semiconductor and (2) separating the conductor from the semiconductor by a sufficient distance to reduce metal-induced gap states (MIGS).

The abstract of the '423 Patent provides:

> An electrical device in which an interface layer is disposed between and in contact with a metal and a Si-based semiconductor, the interface layer being of a thickness effective to depin of the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor. The interface layer may include a layer of a passivating material (e.g., made from nitrogen, oxygen, oxynitride, arsenic, hydrogen and/or fluorine) and sometimes also includes a separation layer. In some cases, the interface layer may be a monolayer of a semiconductor passivating material. The interface layer thickness corresponds to a

[2] The patents share a substantially similar specification (outside the claim set) and the Court cites the '423 Patent herein with the understanding that all the patents include the cited material.

> minimum specific contact resistance of less than or equal to 10 Ω-μm$^2$ or even less than or equal to 1 Ω-μm$^2$ for the electrical device.

The abstract of the ’336 Patent provides:

> An electrical device in which an interface layer comprising arsenic is disposed between and in contact with a conductor and a semiconductor. In some cases, the interface layer may be a monolayer of arsenic.

The abstracts of the ’261, ’167, ’691, and the ’395 Patents are identical and provide:

> An electrical device in which an interface layer is disposed in between and in contact with a conductor and a semiconductor.

Claims 62 and 63 of the ’423 Patent, exemplary asserted claims, recite as follows (with terms in dispute emphasized):

> **62**. An ***electrical device***, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an ***interface layer having a thickness sufficient to depin a Fermi level of the conductor*** in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistance that is ***generally dependent*** on the workfunction of the conductor.
>
> **63**. The electrical device of claim 62 wherein the interface layer includes a ***passivating material***.

’423 Patent col.22 ll.14–23.

## II. LEGAL PRINCIPLES

### A. Claim Construction

“It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To determine the meaning of the claims, courts start by considering the intrinsic evidence. *Id.* at 1313; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc’ns Grp., Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The intrinsic evidence includes the claims themselves, the

specification, and the prosecution history. *Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. The general rule—subject to certain specific exceptions discussed *infra*—is that each claim term is construed according to its ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the patent. *Phillips*, 415 F.3d at 1312–13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003); *Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014) (quotation marks omitted) ("There is a heavy presumption that claim terms carry their accustomed meaning in the relevant community at the relevant time.") *cert. granted, judgment vacated*, 135 S. Ct. 1846 (2015).

"The claim construction inquiry . . . begins and ends in all cases with the actual words of the claim." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998). "[I]n all aspects of claim construction, 'the name of the game is the claim.'" *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1298 (Fed. Cir. 2014) (quoting *In re Hiniker Co.*, 150 F.3d 1362, 1369 (Fed. Cir. 1998)) *overruled on other grounds by Williamson v. Citrix Online, LLC*, 792 F.3d 1339 (Fed. Cir. 2015). First, a term's context in the asserted claim can be instructive. *Phillips*, 415 F.3d at 1314. Other asserted or unasserted claims can also aid in determining the claim's meaning, because claim terms are typically used consistently throughout the patent. *Id.* Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.'" *Id*. (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id*. (quoting *Vitronics Corp. v.*

*Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. *Phillips*, 415 F.3d at 1316. In these situations, the inventor's lexicography governs. *Id*. The specification may also resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." *Teleflex, Inc.*, 299 F.3d at 1325. But, "'[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.'" *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

The prosecution history is another tool to supply the proper context for claim construction because, like the specification, the prosecution history provides evidence of how the U.S. Patent and Trademark Office ("PTO") and the inventor understood the patent. *Phillips*, 415 F.3d at 1317. However, "because the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Id.* at 1318; *see also Athletic Alts., Inc. v. Prince Mfg.*, 73 F.3d 1573, 1580 (Fed. Cir. 1996) (ambiguous prosecution history may be "unhelpful as an interpretive resource").

Although extrinsic evidence can also be useful, it is "'less significant than the intrinsic record in determining the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id*. at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition are not helpful to a court. *Id*. Extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id*. The Supreme Court has explained the role of extrinsic evidence in claim construction:

> In some cases, however, the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period. *See, e.g., Seymour v. Osborne*, 11 Wall. 516, 546 (1871) (a patent may be "so interspersed with technical terms and terms of art that the testimony of scientific witnesses is indispensable to a correct understanding of its meaning"). In cases where those subsidiary facts are in dispute, courts will need to make subsidiary factual findings about that extrinsic evidence. These are the "evidentiary underpinnings" of claim construction that we discussed in *Markman*, and this subsidiary factfinding must be reviewed for clear error on appeal.

*Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 331–32 (2015).

### B. Departing from the Ordinary Meaning of a Claim Term

There are "only two exceptions to [the] general rule" that claim terms are construed according to their plain and ordinary meaning: "1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of the claim term either in the

specification or during prosecution."[3] *Golden Bridge Tech., Inc. v. Apple Inc.*, 758 F.3d 1362, 1365 (Fed. Cir. 2014) (quoting *Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)); *see also GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("[T]he specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal."). The standards for finding lexicography or disavowal are "exacting." *GE Lighting Sols.*, 750 F.3d at 1309.

To act as his own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term," and "clearly express an intent to define the term." *Id*. (quoting *Thorner*, 669 F.3d at 1365); *see also Renishaw*, 158 F.3d at 1249. The patentee's lexicography must appear "with reasonable clarity, deliberateness, and precision." *Renishaw*, 158 F.3d at 1249.

To disavow or disclaim the full scope of a claim term, the patentee's statements in the specification or prosecution history must amount to a "clear and unmistakable" surrender. *Cordis Corp. v. Bos. Sci. Corp.*, 561 F.3d 1319, 1329 (Fed. Cir. 2009); *see also Thorner*, 669 F.3d at 1366 ("The patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope."). "Where an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

### C. Definiteness Under 35 U.S.C. § 112, ¶ 2 (pre-AIA) / § 112(b) (AIA)

Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. A claim, when viewed in light of the intrinsic evidence, must

[3] Some cases have characterized other principles of claim construction as "exceptions" to the general rule, such as the statutory requirement that a means-plus-function term is construed to cover the corresponding structure disclosed in the specification. *See, e.g., CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1367 (Fed. Cir. 2002).

"inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). If it does not, the claim fails § 112, ¶ 2 and is therefore invalid as indefinite. *Id.* at 901. Whether a claim is indefinite is determined from the perspective of one of ordinary skill in the art as of the time the application for the patent was filed. *Id.* at 911. As it is a challenge to the validity of a patent, the failure of any claim in suit to comply with § 112 must be shown by clear and convincing evidence. *BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1365 (Fed. Cir. 2017). "[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012).

When a term of degree is used in a claim, "the court must determine whether the patent provides some standard for measuring that degree." *Biosig Instruments, Inc. v. Nautilus, Inc.*, 783 F.3d 1374, 1378 (Fed. Cir. 2015) (quotation marks omitted). Likewise, when a subjective term is used in a claim, "the court must determine whether the patent's specification supplies some standard for measuring the scope of the [term]." *Datamize, LLC v. Plumtree Software, Inc.*, 417 F.3d 1342, 1351 (Fed. Cir. 2005). The standard "must provide objective boundaries for those of skill in the art." *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014).

## III. AGREED CONSTRUCTIONS

The parties have agreed to constructions set forth in their P.R. 4-5(d) Joint Claim Construction Chart (Dkt. No. 75). Based on the parties' agreement, the Court hereby adopts the agreed constructions for this case.

## IV. CONSTRUCTION OF DISPUTED TERMS

### A. "an electrical device" and "a semiconductor device"

| Disputed Term[4] | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "an electrical device"<br>• '423 Patent Claim 62 | The preamble is limiting. | The preamble is not limiting. |
| "a semiconductor device"<br>• '395 Patent Claim 23 | The preamble is limiting. | The preamble is not limiting. |

Because the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: Giving limiting weight to the "device" preambles is necessary to distinguish between claims expressly drawn to electrical junctions and claims expressly drawn to devices that include such junctions. The distinction between a junction and a device incorporating a junction is repeatedly stated in the Asserted Patents. As described in the patents, the purpose of the invention was to improve electrical and semiconductor devices, not simply to improve a junction. The claim bodies alone do not capture the "device" aspect of the invention, but rather recite simply a junction. The "device" claims are properly understood only with reference to the preambles, and thus the preambles are limiting. Dkt. No. 65 at 4–10.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent, at [54] Title, [57] Abstract, figs.5, 6, 8, col.1 ll.18–19, col.2 l.65 – col.3 l.4, col.3 ll.34–40, col.4 ll.63–66, col.6 ll.6–10, col.7 l.54 –

[4] For all term charts in this order, the claims in which the term is found are listed with the term but: (1) only the highest-level claim in each dependency chain is listed, and (2) only claims identified in the parties' P.R. 4-5(d) Joint Claim Construction Chart (Dkt. No. 75) are listed.

col.8 l.6, col.8 ll.23–32, col.8 ll.56–58, col.9 ll.1–9, col.10 ll.32–35, col.13 ll.12–20, col.15 l.66 – col.16 l.15, col.17 ll.12–18. **Extrinsic evidence**: Piner Decl.[5] ¶¶ 41–47 (Plaintiff's Ex. G, Dkt. No. 65-8).

Defendants respond: Each of the bodies of the claims at issue recites a structurally complete invention and thus the preambles are nonlimiting statements of intended use. As described in the Asserted Patents, the essence of the invention is the metal–interface layer–semiconductor junction. As this essence is expressly recited in the body of the claims at issue, reference to their preambles is not necessary for a proper understanding of the claimed invention. Dkt. No. 69 at 1–4.

In addition to the claims themselves, Defendants cite the following **intrinsic evidence** to support their position: '423 Patent fig.6, col.1 ll.19–22, col.3 ll.56–60, col.4 ll.3–9, col.4 ll.43–46, col.13 ll.11–14.

Plaintiff replies: As described in the Asserted Patents, the invention is not directed solely to a particular junction. It is expressly also directed to devices that include such a junction. The preambles distinguish between claims drawn to devices from those drawn solely to junctions. Dkt. No. 71 at 1.

Plaintiff cites further **intrinsic evidence** to support its position: '423 Patent col.1 ll.18–22.

**Analysis**

The issue in dispute is whether the preambles of Claim 62 of the '423 Patent and Claim 23 of the '395 Patent are limiting. They are not.

Under Federal Circuit precedent "a preamble is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention." *Acceleration Bay, LLC v. Activision Blizzard, Inc.*, 908 F.3d 765,

[5] Declaration of Edwin Piner, Ph.D., Regarding Claim Construction.

770 (Fed. Cir. 2018) (quotation marks and citations omitted). Likewise, a preamble is not limiting when it "merely gives a descriptive name to the set of limitations in the body of the claim that completely set forth the invention." *Am. Med. Sys. v. Biolitec, Inc.*, 618 F.3d 1354, 1359 (Fed. Cir. 2010) (citation omitted). A preamble is limiting, however, when it is "necessary to give life, meaning, and vitality to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002) (quotation marks and citation omitted). For example, "dependence on a particular disputed preamble phrase for antecedent basis may limit claim scope because it indicates a reliance on both the preamble and claim body to define the claimed invention." *Id*. (citation omitted). "Likewise, when the preamble is essential to understand limitations or terms in the claim body, the preamble limits claim scope." *Id*. (citation omitted). "Further, when reciting additional structure or steps underscored as important by the specification, the preamble may operate as a claim limitation." *Id*. (citations omitted).

Here, the preambles at issue do not provide context necessary to properly understand the claims and do not recite any additional limitations over the body of the claim. Claim 62 of the '432 Patent provides:

> **62.** An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction yet thin enough to provide the junction with a specific contact resistance that is generally dependent on the workfunction of the conductor.

'423 Patent col.22 ll.14–21. Claim 23 of the '395 Patent provides:

> **23**. A semiconductor device, comprising:
> a semiconductor region,
> a metal electrical contact to said semiconductor region, and
> an interface layer disposed between and in contact with said semiconductor region and said metal electrical contact, said semiconductor region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising an oxide of titanium and an oxide of the semiconductor region.

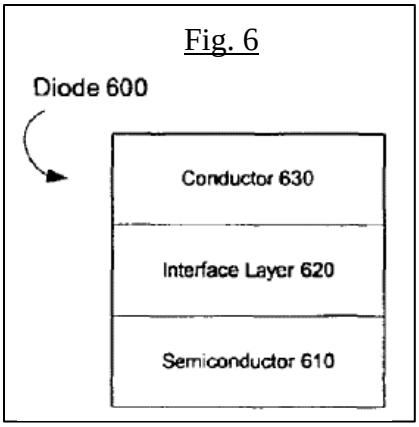
'395 Patent col.20 ll.9–19. Both claims recite a semiconductor-conductor/metal junction with an interface layer disposed between the semiconductor and conductor. The claims further recite that the junction has particular electrical characteristics.

The patents describe that a junction itself is an electrical/semiconductor device. For instance, in describing the prior art, the patents provide:

> One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow).

'423 Patent col.1 ll.25–34. In other words, a semiconductor-metal junction is a device. Similarly, in describing an embodiment of the invention with reference to Figure 6 (reproduced here), the patents provide:

> FIG. 6 shows an example of a diode 600 containing, according to one embodiment of the present invention, an interface layer 620 disposed between and attached to both a semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620.




*Id*. at col.13 ll.11–20. In this embodiment, the conductor-interface layer-semiconductor junction is a device (a diode). While the embodiment here is described with certain electrical characteristics (e.g., it conducts current through a passivated semiconductor surface), the claims at issue themselves recite similar electrical characteristics: Claim 62 of the '423 Patent recites "depin a Fermi level" and "specific contact resistance." Claim 23 of the '395 Patent recites "semiconductor region being electrically connected to said metal electrical contact through said interface."

On balance, the preambles do not provide any important "electrical" or "semiconductor" context that is not stated in the body of the claim. Rather, "electrical device" and "semiconductor device" each "merely gives a descriptive name to the set of limitations in the body of the claim that completely set forth the invention." *Am. Med. Sys.*, 618 F.3d at 1359.

Accordingly, the Court determines that the preambles of Claim 62 of the '423 Patent and Claim 23 of the '395 Patent are not limiting.

### B. The "Depin" Terms

| Disputed Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "sufficiently thick to depin a Fermi level of the semiconductor"<br><br>• '336 Patent Claims 5, 68 | displacing the semiconductor from the contact metal by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminating all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present | displacing the semiconductor from the contact metal by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminating all or substantially all dangling bonds at the surface of the semiconductor |
| "having a thickness sufficient to depin a Fermi level of the conductor"<br><br>• '423 Patent Claim 62<br>• '336 Patent Claims 13, 74, 77 | displacing the semiconductor from the conductor by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminating all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present | displacing the semiconductor from the conductor by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminating all or substantially all dangling bonds at the surface of the semiconductor |

| Disputed Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "has a thickness sufficient to depin a Fermi level of the metal electrical contact"<br><br>• '395 Patent Claim 5 | displaces the semiconductor from the metal electrical contact by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminates all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present | displaces the semiconductor from the metal electrical contact by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminates all or substantially all dangling bonds at the surface of the semiconductor |

Because the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: Depinning with an interface layer is defined in the Asserted Patents as including termination of "all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface . . . ." Dkt. No. 65 at 11 (quoting '423 Patent col.3 ll.23–28) (emphasis removed). This refers to dangling bonds that may be present at the semiconductor surface when the interface layer is not present. *Id*. at 10–12.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent fig.5, col.3 ll.23–28, col.5 ll.1–4, col.9 ll.22–26. **Extrinsic evidence**: Piner Decl. ¶¶ 48–58 (Plaintiff's Ex. G, Dkt. No. 65-8).

Defendants respond: The definition of depinning in the Asserted Patents requires that "all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated …." Dkt. No. 69 at 5 (quoting '423 Patent col.3 ll.23–38) (ellipsis in original). This means simply that all or substantially all of the dangling bonds at the surface have been terminated, otherwise depinning is not achieved. *Id*. at 4–8.

In addition to the claims themselves, Defendants cite the following **intrinsic evidence** to support their position: '423 Patent fig.5, col.3 ll.23–28, col.5 ll.1–4, col.9 ll.21–26, col.9 ll.38–46, col.10 ll.9–26, col.12 ll.21–27, col.15 ll.48–51.

Plaintiff replies: As described in the Asserted Patents, the interface layer serves to improve a metal-semiconductor junction by depinning the semiconductor. This means that the dangling bonds that are terminated by the interface layer are those that would otherwise be present in the junction absent the layer. "If the metal at the metal-semiconductor junction already acts to terminate some dangling bonds, then the interface layer only constitutes an improvement if it terminates more dangling bonds." Dkt. No. 71 at 2; *see also id*. at 1–3.

Plaintiff cites further **intrinsic evidence** to support its position: '423 Patent col.3 ll.12–28, col.4 l.63 – col.5 l.6.

**Analysis**

The issue in dispute distills to whether the patents' statement that "all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface" refers to dangling bonds that may be present if not for the interface layer. It does.

The Court agrees with Plaintiff's interpretation of the "depinning" definitional language. Specifically, the Asserted Patents provide:

> The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is ***a thickness that allows for depinning the Fermi level of the semiconductor*** while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). ***By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated***, and the effect of MIGS has been overcome, or at least reduced, by

> ***displacing* the semiconductor a sufficient distance from the metal**. Minimum specific contact resistances of less than or equal to approximately 10 Ω-μm$^2$ or even less than or equal to approximately 1 Ω-μm$^2$ may be achieved for such junctions in accordance with the present invention.

'423 Patent col.3 ll.12–32 (emphasis added). Thus, depinning involves terminating dangling bonds. Plaintiff's interpretation of the "may otherwise be present" language is more reasonable than Defendants' understanding. Specifically, "depinning" here necessarily includes the addition of a layer to: (1) displace the semiconductor from the metal to reduce MIGS, and (2) terminate bonds that may otherwise be present. There are two relative terms here: "reduced" and "may otherwise be present." These most naturally align with the condition of the junction absent the layer as opposed to stating an alternative to depinning.

Accordingly, the Court construes the "Depin" terms as follows:

- "sufficiently thick to depin a Fermi level of the semiconductor" means "displacing the semiconductor from the contact metal by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminating all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present";
- "having a thickness sufficient to depin a Fermi level of the conductor" means "displacing the semiconductor from the conductor by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap states in the semiconductor and terminating all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present";
- "has a thickness sufficient to depin a Fermi level of the metal electrical contact" means "displaces the semiconductor from the metal electrical contact by a sufficient distance to eliminate or at least reduce the effects of metal-induced gap

states in the semiconductor and terminates all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present."

### C. "passivating material"

| Disputed Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "passivating material"<br>• '423 Patent Claim 63 | plain and ordinary meaning | material that terminates all or substantially all dangling bonds at the surface of the semiconductor |

**The Parties' Positions**

Plaintiff submits: The claim at issue does not require passivation, it simply requires a "passivating material." Rather, "passivating material" is used in the claim at issue as "passivation material" is used in the description, according to its plain and ordinary meaning. Dkt. No. 65 at 12–13.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent col.3 ll.39–52, col.3 l.67 – col.4 l.2, col.5 ll.1–6, col.8 ll.11–12, col.8 ll.40–43, col.9 ll.40–42, col.9 ll.60–67, col.10 ll.47–50, col.12 ll.56–61. **Extrinsic evidence**: Neil Sclater and John Markus, *McGraw-Hill Electronics Dictionary* at 329 (6th ed. 1997), "passivation" (Plaintiff's Ex. K, Dkt. No. 65-12 at 4); *McGraw Hill Dictionary of Scientific and Technical Terms* (6th ed. 2003), "passivation" (Plaintiff's Ex. L, Dkt. No. 65-13 at 4); *Modern Dictionary of Electronics* at 542 (7th ed. 1999), "passivation" (Plaintiff's Ex. M, Dkt. No. 65-14 at 4).

Defendants respond: The Asserted Patents define "passivate" and "passivation" as eliminating or terminating dangling bonds. Dkt. No. 69 at 8–9 (citing '423 Patent col.5 ll.1–6, col.9 ll.23–26). Thus, the "passivating material," which is material defined by its passivating function, must

terminate the all or substantially all dangling bonds. Indeed, Plaintiff's expert states as much. *Id*. at 10 (citing Piner Decl. ¶¶ 59–60). *Id*. at 8–10.

In addition to the claims themselves, Defendants cite the following intrinsic and extrinsic evidence to support their position: **Intrinsic evidence**: '423 Patent col.5 ll.1–6, col.9 ll.23–26. **Extrinsic evidence**: Piner Decl. ¶¶ 59–60 (Plaintiff's Ex. G, Dkt. No. 65-8).

Plaintiff replies: Neither Plaintiff's not Defendants' expert initially provided any opinion on the construction of "passivating material." Rather, the experts opined on the dispute over the dangling bonds that are terminated by the interface layer, which dispute is presented in the Depin terms. During claim-construction discovery, it became apparent that the "passivating material" should not be construed to incorporate the definition of the depinning that applies to the interface layer. Indeed, doing so would eliminate any distinction between Claim 63 of '423 Patent and Claim 62 from which Claim 63 depends. Further, "passivating material" should not be interpreted the same as "passivating layer." Dkt. No. 71 at 4–5.

Plaintiff cites further intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent col.3 ll.12–28. **Extrinsic evidence**: Piner Decl. ¶ 60 (Plaintiff's Ex. G, Dkt. No. 65-8); Bokor Decl. (Plaintiff's Ex. I, Dkt. No. 65-10); Piner Dep.[6] at 261:23 – 262:6, 264:3–15. 265:7–11, 266:18 – 268:13 (Plaintiff's Ex. W, Dkt. No. 71-2 at 40–41, 43–47).

**Analysis**

The issue in dispute is whether the "passivating material" must terminate all or substantially all of the dangling bonds at the semiconductor surface. The material must be capable of terminating dangling bonds at the surface of the semiconductor, but it need not terminate all or substantially all such bonds as Defendants propose.

[6] Remote Videotaped Deposition of Edwin Piner Ph.D.

The Asserted Patents use "passivating material" to refer to a material used to build a layer rather than a layer itself. For instance, the patents provide:

> The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be ***essentially a monolayer*** (or several monolayers) ***of a semiconductor passivating material***.
>
> In another embodiment, the interface layer is made up of ***a passivation layer*** fabricated by heating the semiconductor in the presence of nitrogenous ***material***, for example ammonia ($NH_3$), nitrogen ($N_2$) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface ***layer may be fabricated*** by heating the semiconductor while in a vacuum chamber and ***exposing the semiconductor to the nitrogenous material***.

'423 Patent col.3 ll.41–55 (emphasis added). This describes that the "passivating material" is the building block of the passivation layer. The patents similarly provide:

> A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, ***exposing a silicon surface to oxygen*** (under the appropriate conditions to ***grow a protective film of silicon dioxide***) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated.

*Id*. at col.8 ll.9–18. Again, this suggests that a layer (or "film") is constructed of the material rather than being coextensive with the material. *See also id*. at col.8 ll.51–55 ("In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.").

The passivating material terminates (bonds with) dangling bonds on the surface of the semiconductor but it is the passivating layer that terminates all (or substantially all) of the dangling bonds that would otherwise be there. For example, the patents describe:

> The interface layer 520 is formed on the semiconductor 530 and may contain a ***passivation material that bonds to the semiconductor material*** by way of a covalent (or other) bond formed between the passivation material and the

> semiconductor material. For example, ***an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom*** to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer 520**,** while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation layer. That is, ***the interface layer serves to*** (i) chemically ***passivate the semiconductor surface*** 540**,** and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS.

*Id*. at col.9 ll.39–53 (emphasis added).; *see also id*. at col.8 ll.9–18 (describing the formation of the "protective film" on the surface); *id*. at col.5 ll.1–6 ("The interface layer functions to ***passivate the semiconductor surface*** (***that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface***) and to displace the semiconductor from the metal so as to reduce the effect of MIGS." (emphasis added)).

The use of "passivating material" to denote material that is capable of bonding with dangling bonds comports with a customary meaning of "passivation." *See, e.g.*, *Modern Dictionary of Electronics* at 542 (7th ed. 1999) (defining "passivation" as "[e]lectrical treatment of a metal or semiconductor to create a chemically bonded oxide layer on the surface to protect it from corrosion"). Dkt. No. 65-14 at 4.

On balance, Defendants' proposed construction is more applicable to a passivating layer than it is to the material used to build the layer and Plaintiff's "plain and ordinary" meaning construction threatens to capture a myriad of dictionary definitions that do not properly reflect the use of the "passivating material" in the patents.

Accordingly, the Court construes "passivating material" as follows:

- "passivating material" means "material capable of terminating dangling bonds at the surface of the semiconductor."

### D. The "Interface Layer" Terms

| Disputed Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "interface layer"<br><br>• '423 Patent Claim 62<br>• '336 Patent Claims 1, 5, 9, 13, 65, 68, 71, 74, 77<br>• '261 Patent Claims 1, 21<br>• '167 Patent Claim 1<br>• '691 Patent Claim 25<br>• '395 Patent Claims 1, 17, 23 | plain and ordinary meaning | a layer of material, other than metal silicide, at the interface between the [conductor, contact metal, metal electrical contact] and the semiconductor |
| "wherein the interface layer further includes a separation layer"<br><br>• '423 Patent Claim 66 | wherein the interface layer includes a layer of material, distinct from a layer including the passivating material, to further displace the conductor from the semiconductor | aside from "interface layer," addressed above, agree with Acorn's construction |
| "the interface layer comprising a metal oxide and an oxide of the semiconductor"<br><br>• '167 Patent Claim 1 | the interface layer comprising a layer of a metal oxide and a distinct layer of an oxide of the semiconductor | aside from "interface layer," addressed above, agree with Acorn's construction |
| "said interface layer comprising a metal oxide and a semiconductor oxide"<br><br>• '395 Patent Claim 1 | said interface layer comprising a layer of a metal oxide and a distinct layer of a semiconductor | aside from "interface layer," addressed above, agree with Acorn's construction |
| "said interface layer comprising an oxide of titanium and an oxide of the semiconductor"<br><br>• '395 Patent Claim 17 | said interface layer comprising a layer of an oxide of titanium and a distinct layer of an oxide of the semiconductor | aside from "interface layer," addressed above, agree with Acorn's construction |

| Disputed Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "said interface layer comprising an oxide of titanium and an oxide of the semiconductor region"<br><br>• '395 Patent Claim 23 | said interface layer comprising a layer of an oxide of titanium and a distinct layer of an oxide of the semiconductor region | aside from "interface layer," addressed above, agree with Acorn's construction |

Because the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff submits: It would be improper to exclude "metal silicide" from the scope of "interface layer." While the Asserted Patents include criticism of an interface layer comprised solely of metal silicide, the patents allow a multi-component interface layer. This means that even if an interface layer consisting solely of a metal silicide may not achieve the purpose of the invention, the interface layer of the claims may include a metal silicide. In fact, the patents disclose that the conductor of the junction ***may*** be one that is not able to form a silicide, implying that it may be one that does form a silicide. Dkt. No. 65 at 15–16 (citing '423 Patent col.15 ll.18–27). Further, the patents disclose use of metals that are known to form silicides. *Id*. at 16 (citing '423 Patent col.13 ll.56–65). Finally, Claims 17 and 19 of the '261 Patent expressly recite negative limitations directed at silicides, indicating that it would be improper to include such a negative limitation when it is not expressed. *Id*. at 13–17.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent, at [57] Abstract, col.13 ll.56–65, col.14 l.61 – col.15 l.27. **Extrinsic evidence**: Piner Decl. ¶¶ 61–74 (Plaintiff's Ex. G, Dkt. No. 65-8).

Defendants respond: The Asserted Patents include a disclaimer of metal silicide in the interface layer. Specifically, the patents disparage the prior-art approach of using silicide-forming metals at the contact with the semiconductor. The use of metal silicides in electrical junctions that is disclosed in the patents is restricted to the conductor—the patents do not disclose use of a metal silicide at the interface layer. Rather, they teach that putting a metal silicide at the surface of semiconductor would cause MIGS, which runs counter to the purpose of the invention. Claims 17 and 19 of the '261 Patent do not suggest using a metal silicide in the interface layer: Claim 17 is expressly directed to the "contact metal" and "[t]here is no dispute that the 'contact metal' is the conductor and is not part of the interface layer." Dkt. No. 69 at 14. Claim 19 is directed to a "barrier layer" rather than an "interface layer." *Id*. at 10–15.

In addition to the claims themselves, Defendants cite the following intrinsic and extrinsic evidence to support their position: **Intrinsic evidence**: '423 Patent, at [54] Title, [57] Abstract, fig.6, col.1 ll.18–22, col.2 ll.35–42, col.2 l.65 – col.3 l.9, col.3 ll.11–28, col.4 ll.43–47, col.5 ll.1–6, col.7 l.46 – col.8 l.6, col.12 ll.56–66, col.13 ll.26–30, col.14 l.61 – col.15 l.27. **Extrinsic evidence**: Piner Dep. at 64:14–17, 75:14 – 77:4, 88:6–11, 88:23 – 89:20 (Defendants' Ex. 1, Dkt. No. 69-2 at 17–22).

Plaintiff replies: As explained in the Asserted Patents, one of the benefits of the invention is that it allows for contact metals other than those that can form a silicide. Dkt. No. 71 at 6 (citing '423 Patent col.12 ll.56–66). But this does not preclude the use of silicide-forming metals at the interface. In fact, the patents teach that a metal silicide may be suitable as a passivating layer, allowing the silicide to be combined with a separation layer to address MIGS and thereby form an interface layer of the claims. Finally, the patents do not require an interface layer to reduce MIGS.

When required, such a limitation is expressed in the claims through reference to depinning, MIGS, or specific materials. Dkt. No. 71 at 5–7.

Plaintiff cites further intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent col.12 ll.56–66. **Extrinsic evidence**: Piner Dep.[7] at 74:12 – 75:2, 77:7–10, 88:17–21 (Plaintiff's Ex. W, Dkt. No. 71-2 at 35–36, 38–39).

**Analysis**

The issue in dispute is whether the claims exclude any metal silicide from the interface layer. They do not.

The discussion of metal silicide in the Asserted Patents does not rise to a disclaimer of metal silicide in the interface layer. As described in the patents, one prior-art approach to tuning the Schottky barrier height involved the use of a silicide at the contact of the conductor with the semiconductor. For example, the patents provide:

> As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by ***forming an interface layer*** (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) ***between a metal and a semiconductor***. ***This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal*** (and thus limiting the choices of available contact metals to those that can form suicides), or using esoteric substrates that exhibit wide bandgaps.

'423 Patent col.12 ll.56–66 (emphasis added). This explains that placing a layer between the contact metal (conductor) and the semiconductor differs from using a silicide as the contact metal in a junction lacking any layer between the contact metal and semiconductor.

Elsewhere, the patents suggest using a metal silicide as the contact metal in an embodiment that includes an interface layer:

[7] Remote Videotaped Deposition of Edwin Piner Ph.D.

> FIG. 6 shows an example of a diode 600 containing, according to one embodiment of the present invention, an interface layer 620 disposed between and attached to both a semiconductor 610 and a conductor 630. …
>
> The ***conductor*** 630 contains a conductive material such as a metal or an alloy of a metal. … Unless otherwise specified, ***conductors include*** metals (e.g., pure metals and alloys), and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and ***metal silicides***.

*Id*. at col.13 ll.11–33 (emphasis added). Thus, the claims do not necessarily exclude a junction in which the conductor is a metal silicide and is separated from the semiconductor by an interface layer. But the invention need not be implemented using a silicide-forming metal as the contact metal because the interface layer provides passivation:

> Another advantage achieved through the use of the interface layer 620 is greater flexibility afforded in selecting a conductor 630. Typically, metals chosen for application in ***classic Schottky diodes*** are those that can form a silicide with a silicon semiconductor. ***The formation of the silicide helps to reduce surface states (resulting, from dangling bonds), but not the effects of MIGS***. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.
>
> According to one embodiment of the present invention, ***however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed*** because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

*Id*. at col.15 ll.6–28 (emphasis added). In other words, the passivating effect of the metal silicide at the contact is neither necessary nor sufficient to depin the Fermi level in the conventional approach. To depin, a layer is inserted between the conductor and the semiconductor and thus the conductor is not limited to a metal silicide. *See id*. at col.17 ll.14–52 (contrasting a silicide-semiconductor junction of the prior art with a metal-interface layer-semiconductor junction of the invention).

Taken together, these teachings establish that a metal silicide-semiconductor junction was in the prior art and is distinct from the metal-interface layer-semiconductor junction of the invention. But this does not unambiguously establish that no metal silicide may be present in the interface layer. Indeed, these disclosures teach that a metal silicide passivates the semiconductor (reducing surface states that result from dangling bonds). The patents further teach multi-component interface layers: "The interface layer may include a passivating material . . . and sometimes also includes a separation layer." *Id*. at col.3 ll.41–44. Thus, it is conceivable that an interface layer may include a metal silicide as a passivating material in addition to a separation layer to achieve depinning. A metal-interface layer-semiconductor junction with such a compound interface layer would not be the same as the disparaged prior-art silicide-semiconductor junction, which lacks an interface layer.

Accordingly, the Court rejects Defendants' other-than-metal-silicide negative limitation, determines that "interface layer" has its plain and ordinary meaning without the need for further construction, and construes the remaining terms as follows:

- "wherein the interface layer further includes a separation layer" means "wherein the interface layer includes a layer of material, distinct from a layer including the passivating material, to further displace the conductor from the semiconductor";
- "the interface layer comprising a metal oxide and an oxide of the semiconductor" means "the interface layer comprising a layer of a metal oxide and a distinct layer of an oxide of the semiconductor";
- "said interface layer comprising a metal oxide and a semiconductor oxide" means "said interface layer comprising a layer of a metal oxide and a distinct layer of a semiconductor";

- "said interface layer comprising an oxide of titanium and an oxide of the semiconductor" means "said interface layer comprising a layer of an oxide of titanium and a distinct layer of an oxide of the semiconductor"; and
- "said interface layer comprising an oxide of titanium and an oxide of the semiconductor region" means "said interface layer comprising a layer of an oxide of titanium and a distinct layer of an oxide of the semiconductor region."

### E. "a metal oxide layer, and a passivating dielectric tunnel barrier layer" and "the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer"

| Disputed Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "a metal oxide layer, and a passivating dielectric tunnel barrier layer"<br>• '691 Patent Claim 1 | a metal oxide layer, and a distinct dielectric tunnel barrier layer that terminates all or substantially all dangling bonds that may be present at the surface of the semiconductor region without the layer present | a metal oxide layer, and a distinct dielectric tunnel barrier layer that terminates all or substantially all dangling bonds at the surface of the semiconductor region |
| "the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer"<br>• '691 Patent Claim 25 | the interface layer comprising a metal oxide separation layer and a distinct layer of a semiconductor oxide that terminates all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present | the interface layer comprising a metal oxide separation layer and a distinct layer of a semiconductor oxide that terminates all or substantially all dangling bonds at the surface of the semiconductor |

Because the parties' arguments and proposed constructions with respect to these terms are related, the Court addresses the terms together.

**The Parties' Positions**

Plaintiff and Defendants submit that the issues in dispute regarding these terms are the same as presented in the Depin terms. Dkt. No. 65 at 17–18; Dkt. No. 69 at 15.

**Analysis**

For the reasons set forth in regard to the "Depin" terms, the Court construes these terms as follows:

- "a metal oxide layer, and a passivating dielectric tunnel barrier layer" means "a metal oxide layer, and a distinct dielectric tunnel barrier layer that terminates all or substantially all dangling bonds that may be present at the surface of the semiconductor region without the layer present"; and
- "the interface layer comprising a metal oxide separation layer and a semiconductor oxide passivation layer" means "the interface layer comprising a metal oxide separation layer and a distinct layer of a semiconductor oxide that terminates all or substantially all dangling bonds that may be present at the surface of the semiconductor without the layer present."

**F. "configured to"**

| Disputed Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "configured to"<br><br>• '336 Patent Claims 1, 65<br>• '261 Patent Claim 1<br>• '691 Patent Claim 20 | plain and ordinary meaning | "designed to" |

**The Parties' Positions**

Plaintiff submits: Defendants provide no evidence to justify construing "configured to" as "designed to." Dkt. No. 65 at 18–19.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent col.13 ll.31–34. **Extrinsic**

**evidence**: Bokor Dep. at 147:10–21 (Plaintiff's Ex. J, Dkt. No. 65-11 at 15); Piner Decl. ¶ 90 (Plaintiff's Ex. G, Dkt. No. 65-8).

Defendants respond: In the context of the surrounding claim language and description of the invention, "configured to" refers to an interface layer "designed with an appropriate thickness to depin the Fermi level and reduce the Schottky height barrier" rather than one that is "merely capable of reducing the height of the Schottky barrier." Dkt. No. 69 at 17; *see also id*. at 16–18.

In addition to the claims themselves, Defendants cite the following **intrinsic evidence** to support their position: '423 Patent col.7 l.37 – col.8 l.6, col.15 ll.43–47.

Plaintiff replies: That a layer is "configured to" reduce the height of the Schottky barrier height is not a statement of some theoretical capability to do such but is a statement that it actually does such. Whether the layer does reduce the barrier height does not properly involve exploring the intent of the product designers, as Defendants' construction supposes. Dkt. No. 71 at 7–8.

**Analysis**

The issue in dispute appears to distill to whether a layer that is "configured to" reduce a Schottky barrier height is necessarily intentionally designed for that purpose. It is not.

The Court rejects Defendants' proposed construction. Defendants have not identified any evidence that rises to the exacting standard required to redefine the plain meaning of "configured to" as "designed to." Plaintiff is not advocating mere capability, so Defendants' construction appears to address a non-issue and therefore fails to clarify anything. Further, Defendants' construction threatens to improperly supplant a component's role in a particular system with the component-creator's subjective intent for the component, perhaps divorced from the system. For example, a particular layer designed for structural purposes may also incidentally possess passivation attributes. Such a layer may not be "designed to" "reduce a height of a Schottky barrier

. . . ," but can, in fact, be used to reduce the height of the barrier. Thus, Defendants' proposed "designed to" limitation could improperly exclude a layer that is actually used to reduce the height of the barrier. The Federal Circuit has further instructed that "configured to" does not include a "subjective element" such as the designer's intent. *Cochlear Bone Anchored Sols. AB v. Oticon Med. AB*, 958 F.3d 1348, 1356 (Fed. Cir. 2020) (citations omitted).

Accordingly, the Court rejects Defendants' proposed construction and determines that this term has its plain and ordinary meaning without the need for further construction.

**G. "generally dependent"**

| Disputed Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "generally dependent"<br><br>• '423 Patent Claim 62<br>• '395 Patent Claim 5 | plain and ordinary meaning | indefinite |

**The Parties' Positions**

Plaintiff submits: In the appropriate context, "generally dependent" refers to the relationship between contact resistance and workfunction and denotes "a specific contact resistance that is more dependent on the workfunction of the conductor than was observed in the prior art." Dkt. No. 65 at 24. During prosecution of the '423 Patent, the "generally dependent" language was added and used to distinguish prior art in which the resistance was independent of the workfunction. The Asserted Patents also disclose the dependence of Schottky barrier height on workfunction, and the known relationship between barrier height and contact resistance is one of a complicated dependence, in which contact resistance varies with the square root of the barrier height. To denote such a complicated relationship, "generally dependent" is the appropriate terminology. Further, Samsung Electronics Co. was able to ascertain the meaning of the claim language in *Inter Partes* Review ("IPR"), so the language cannot be indefinite. *Id*. at 19–28.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent fig.8, col.1 ll.38–57, col.1 l.59 – col.3 l.9, col.5 l.24, col.5 l.26, col.6 ll.6–10, col.8 ll.61–62, col.11 l.2, col.11 l.13, col.12 ll.56–61, col.14 ll.9–14, col.15 ll.43–47, col.16 ll.6–9, col.17 l.28; '423 Patent File Wrapper April 4, 2005 Amendment at 10, 12 (Plaintiff's Ex. N, Dkt. No. 65-15 at 13, 15). **Extrinsic evidence**: Piner Decl. ¶¶ 108–19 (Plaintiff's Ex. G, Dkt. No. 65-8); Piner Dep. 53:19 – 55:6 (Plaintiff's Ex.H, Dkt. No. 65-9 at 11–13); Bokor Decl.[8] ¶¶ 22, 24, 26, 28 n.2 (Plaintiff's Ex. I, Dkt. No. 65-10); Bokor Dep. at 33:20 – 35:23, 60:24 – 61:5, 63:24–25, 69:21 – 71:1, 157:12 – 181:24 (Plaintiff's Ex. J, Dkt. No. 65-11 at 4–9, 12–14, 16–40); J. Bokor et al., *Advanced Lithography for ULSI*, IEEE Circuits and Devices Magazine Vol.12, No.1[9] at 12 (Jan. 1996) (Plaintiff's Ex. O, Dkt. No. 65-16 at 3); Dennis Sinitsky et al., *High Field Hole Velocity and Velocity Overshoot in Silicon Inversion Layers*, IEEE Electron Device Letters, Vol.18, No.2 at 54, 56 (Feb. 1997) (Plaintiff's Ex. P, Dkt. No. 65-17 at 2, 4); Yu-Chih Tseng et al., *Effect of Diameter Variation in a Large Set of Carbon Nanotube Transistors*, Nano Lett. Vol.6, No.7 (2006) at 1365–66, 1368 (Plaintiff's Ex. Q, Dkt. No. 65-18 at 3–4); M. Teresa Martinez et al., *Streptavidin as CNTs and DNA Linker for the Specific Electronic and Optical Detection of DNA Hybridization*, J. Phys. Chem. C (2012) at 22584 (Plaintiff's Ex. R, Dkt. No. 65-19 at 7); IPR '423 Petition[10] at 39–45 (Plaintiff's Ex. S, Dkt. No. 65-20 at 3–9); IPR '423 Schubert Decl.[11] at ¶¶ 120–30 (Plaintiff's Ex. T, Dkt. No. 65-21); IPR

[8] Declaration of Jeffrey Bokor, Ph.D.

[9] The document submitted by Plaintiff does not identify the journal, but indicates it was downloaded from IEEE Xplore, which in turn identifies the journal: https://ieeexplore.ieee.org/document/481203.

[10] Petition for *Inter Partes* Review of U.S. Patent No. 7,084,423, *Samsung Elecs. Co. v. Acorn Semi*, LLC, IPR 2020-01182, Paper No. 2 (P.T.A.B. June 24, 2020).

[11] Declaration of Dr. E. Fred Schubert, *Samsung Elecs. Co. v. Acorn Semi, LLC*, IPR 2020-01182, Ex. No. 1003 (P.T.A.B. June 24, 2020).

'395 Petition[12] at 32–34 (Plaintiff's Ex. U, Dkt. No. 65-22 at 3–4); IPR '395 Schubert Decl.[13] at ¶¶ 184–96 (Plaintiff's Ex. V, Dkt. No. 65-23).

Defendants respond: It is not reasonably certain what "generally dependent" means beyond "dependent." But it is certain that it means something other than simply "dependent" else "generally" would have no effect. In the context of the claims at issue, "generally," as it is generally understood, does not convey the precision required to specify the degree to which the contact resistance depends on the workfunction. Additionally, there is no disclosure in the intrinsic record that provides a standard by which to determine this degree. In the IPR, Samsung asserted art that disclosed such a strong dependence between resistance and workfunction that it clearly falls within the scope of "generally dependent," even without reasonable certainty regarding the lower end of the dependence denoted by "generally dependent." Dkt. No. 69 at 18–26.

In addition to the claims themselves, Defendants cite the following intrinsic and extrinsic evidence to support their position: **Intrinsic evidence**: '423 Patent fig.8, col.14 ll.27–50; '423 Patent File Wrapper April 4, 2005 Amendment at 10, 12 (Defendants' Ex. 4, Dkt. No. 69-5 at 13, 15). **Extrinsic evidence**: Bokor Decl. ¶¶ 21–31 (Plaintiff's Ex. I, Dkt. No. 65-10); Piner Decl. ¶¶ 112–17 (Plaintiff's Ex. G, Dkt. No. 65-8); Piner Dep. at 25:19 – 26:1, 35:9 – 36:6, 36:8–17, 39:16 – 40:10, 51:3 – 52:17, 53:19 – 55:6 (Defendants' Ex. 1, Dkt. No. 69-2 at 6–16); Bokor Dep. at 33:20 – 34:16, 160:13 – 162:1 (Defendants' Ex. 2, Dkt. No. 69-3 at 5–6, 8–10); *The American Heritage Dictionary of the English Language* at 732 (4th ed. 2006), "generally" (Defendants' Ex. 3, Dkt. No. 69-4 at 4); IPR '423 Petition at 22 n.2, 39–45 (Defendants' Ex. 5, Dkt. No. 69-6 at 32,

[12] Petition for *Inter Partes* Review of U.S. Patent No. 10,090,395, *Samsung Elecs. Co. v. Acorn Semi, LLC*, IPR 2020-01282, Paper No. 2 (P.T.A.B. July 13, 2020).
[13] Declaration of Dr. E. Fred Schubert, *Samsung Elecs. Co. v. Acorn Semi, LLC*, IPR 2020-01182, Ex. No. 1126 (P.T.A.B. July 13, 2020).

49–55); IPR '423 Schubert Decl. at ¶¶ 120–30 (Defendants' Ex. 6, Dkt. No. 69-7); IPR '395 Petition at 15 n.1, 32–34 (Defendants' Ex.7, Dkt. No. 69-8 at 44–46); IPR '395 Schubert Decl. at ¶¶ 184–96 (Defendants' Ex.8, Dkt. No. 69-9).

Plaintiff replies: Defendants' expert testified that the "generally dependent" language refers to more than "some minimal dependency" else the claims would capture the prior art. Thus, "generally dependent" refers to a dependence that is greater than that known in the prior art. Dkt. No. 71 at 8–10.

Plaintiff cites further intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent col.14 ll.27–50. **Extrinsic evidence**: Piner Dep. at 19:3 – 20:21, 22:15–24, 27:18 – 28:4, 30:8 – 32:5, 36:8 – 46:10 (Plaintiff's Ex. W, Dkt. No. 71-2 at 7–8, 10, 15–16, 18–20, 24–34); Bokor Dep. at 31:11 – 35:23 (Plaintiff's Ex. X, Dkt. No. 71–3 at 4–8); E.H. Rhoderick, *Metal-Semiconductor Contacts*, IEEE PROC., Vol.129, Pt.1 No.1 at fig.2 (Feb. 1982) (Plaintiff's Ex. I,[14] Dkt. No. 65-10 at 76–89, 78).

**Analysis**

The issue in dispute is whether "generally dependent" in the claims refers to a reasonably certain degree of dependence of the specific contact resistance on the workfunction or Fermi energy. It does not.

The term "generally dependent" appears in the claims to relate the specific contact resistance to the workfunction of the conductor or the Fermi energy of the semiconductor. Claim 62 of the '423 Patent provides:

> **62.** An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction yet thin enough to provide the junction

[14] *Roderick* is Exhibit D to the Bokor Decl.

> with a ***specific contact resistance that is <u>generally dependent</u> on the workfunction of the conductor***.

'423 Patent col.22 ll.14–21 (emphasis added). Claim 5 of the '395 Patent provides:

> 5. The electrical junction of claim 1, wherein said interface layer has a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction yet thin enough to provide the junction with ***a specific contact resistivity that is <u>generally dependent</u> on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region***.

'395 Patent col.18 l.62 – col.19 l.3 (emphasis added).

The term "generally dependent" is a term of degree for which the Asserted Patents do not provide sufficient guidance for determining the degree. The Court rejects Plaintiff's position that "generally dependent" in the claims refers to any dependence greater than what was known in the prior art. To begin, nothing in the plain meaning of "generally dependent" invokes a comparison to the prior art, and definitely not to any specific or reasonably certain level of dependence known in the prior art. Plus, there is no disavowal or disclaimer in the patents that would limit the claimed dependence of the specific contact resistance on the workfunction in the way Plaintiff suggests.

The patents describe known relationships between the Schottky barrier height and workfunction (which the parties agree denotes a relationship between contact resistance and workfunction) as: (1) "direct variation" of the barrier height with the work function, (2) a "much weaker variation", and (3) no variation (independence). '423 Patent col.1 l.38 – col.2 l.19. The weaker-than-direct variation is attributed in part to surface states of the semiconductor. *Id*. at col.1 l.65 – col.2 l.19; col.2 ll.61–63. A goal of the invention is to eliminate or reduce the surface-state effects using an interface layer to passivate the semiconductor and remove MIGS in order to allow tuning of the barrier height. *Id*. at col.3 ll.3–9; col.7 ll.46–54; col.9 ll.21–35. In one embodiment, passivation yields "a barrier height that depends predominantly upon the bulk characteristics of

the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer." *Id*. at col.13 ll.41–56. In another embodiment, the interface layer "de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials)." *Id*. at col.15 ll.38–49. "Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used." *Id*. at col.14 ll.16–26. Even if the interface layer is sufficiently thick to remove surface-state effects, the barrier height (and thus contact resistance) may depend on other parameters, such as layer thickness, temperature of layer formation, and layer material. *Id*. at col.14 ll.16–60. But while the patents describe that the barrier height may depend on, or even "predominantly depend" on, a variety of characteristics, there is no description of what it means for the height to "generally depend" on any characteristic.

The intrinsic evidence of record provides that the only clear distinction between the prior-art dependence and the claimed dependence is that "generally dependent" does not encompass "independent." Specifically, "generally dependent" was added during prosecution with the following argument:

> New claim 62 recites an electrical device in which the interface layer has a thickness sufficient to depin a Fermi level of the conductor yet thin enough to provide the junction with a specific contact resistance that is ***generally dependent on the workfunction of the conductor***. Support for this claim may be found, for example at paragraph 70 et seq. of the specification as originally filed. This claim is patentable over Schroen, which specifically indicates that the junction has a thickness sufficiently thick so that resistance is ***independent of the metal workfunction***. *See, e.g.,* Schroen at col. 5, 11, 19–24 ('the metallurgical compatibility constraint is removed."). Because these junctions are thus substantially different, the new claim is patentably distinct from the structure disclosed by Schroen.

'423 Patent File Wrapper April 4, 2005 Amendment at 10, 12 (emphasis in original), Dkt. No. 69-5 at 13, 15. But "dependent" plainly does not encompass "independent." Thus, the import of "generally" is not clear from this distinction.

Exacerbating the lack of reasonable certainty regarding what degree of dependence qualifies as "generally dependent" is a lack of a reasonably certain baseline with which to compare. For instance, it is not clear if "generally dependent" refers to a dependence relative to some level of variation of resistance with metal workfunction (or semiconductor Fermi energy[15]) or to a dependence relative to some level of variation of resistance with, e.g., layer thickness.

Ultimately, the Court declines to interpret the "generally dependent" term of degree as plainly relative to the prior art en masse. The patents do not tie "generally" to any particular level of dependence in the prior art and the only specific distinction made over the prior art is fully found in "dependent." The patents also do not tie "generally dependent" on work function or Fermi energy to any relationship between work function or Fermi energy with any other characteristic, such as layer thickness. Simply, the patents do not sufficiently explain the standard for determining if a particular dependence qualifies as "generally dependent." The claims at issue are not "precise enough to afford clear notice of what is claimed" and therefore fail to "appris[e] the public of what is still open to them." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 909 (2014) (quotation marks omitted) (citations omitted).

Accordingly, Defendants have established that the meaning of "generally dependent" in Claim 62 of the '423 Patent and Claim 5 of the '395 Patent is not reasonably certain, and the Court finds the term "generally dependent" indefinite.

[15] While Claim 5 of the '395 Patent recites a "specific contact resistivity that is generally dependent on: a ***workfunction*** of the metal electrical contact, a ***Fermi energy*** of the semiconductor in the region, or ***both*** the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region," Plaintiff focuses its arguments solely on the relationship between resistivity (resistance) and workfunction. On the record before the Court, there is no sufficiently definite guidance regarding what it means for the contact resistivity to be generally dependent on the Fermi energy.

### H. "the contact metal"

| Disputed Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| "the contact metal"<br>• '261 Patent Claim 23 | the conductor | indefinite (lacks antecedent basis) |

**The Parties' Positions**

Plaintiff submits: The term "the contact metal" in Claim 23 of the '261 Patent refers to the "conductor" in Claim 21, from which Claim 23 depends. Dkt. No. 65 at 28–30.

In addition to the claims themselves, Plaintiff cites the following intrinsic and extrinsic evidence to support its position: **Intrinsic evidence**: '423 Patent, at [57] Abstract, col.1 ll.25–26, col.4 ll.3–9, col.12 ll.56–66, col.13 ll.21–33. **Extrinsic evidence**: Piner Decl. ¶¶ 101–07 (Plaintiff's Ex. G, Dkt. No. 65-8).

Defendants respond: As described in the Asserted Patent, not all conductors are metals. Thus, it is not clear that "the contact metal" refers to the "conductor." Dkt. No. 69 at 26–27.

In addition to the claims themselves, Defendants cite the following intrinsic and extrinsic evidence to support their position: **Intrinsic evidence**: '423 Patent col.13 ll.27–31, col.13 ll.35–42. **Extrinsic evidence**: Piner Decl. ¶¶ 105–06 (Plaintiff's Ex. G, Dkt. No. 65-8).

Plaintiff replies: The use of "contact metal" in Claim 23 is clearly an error. It is meant to refer to the "conductor." Dkt. No. 71 at 10.

**Analysis**

The issue in dispute is whether it is reasonably certain that "the contact metal" in Claim 23 of the '261 Patent refers to the "conductor" in Claim 21. It is not.

The claims at issue are as follows:

> **21.** An electrical junction, comprising ***a conductor***; a semiconductor selected from a list consisting of Si, Ge, C (a crystal structure of which is selected from

> a list comprising a diamond lattice, a fulleride or a polymer), an alloy of Ge and Si, an alloy of Ge and C, an alloy of Si and C, and an alloy of Si, Ge, and C; and an interface layer disposed therebetween, the semiconductor comprising a source or drain of a transistor, and the interface layer comprising a metal oxide and having a thickness of approximately 0.1 nm to 5 nm.
>
> **23.** The electrical junction of claim 21**,** wherein ***the contact metal*** is a metal or a stack of metals deposited on the interface layer.

'261 Patent col.18 l.63 – col.19 l.4; *id*. at col.19 l.8–10 (emphasis added). It is not reasonably certain that reference to "the contact metal" in Claim 23 refers to the "conductor" in Claim 21. As explained in the Asserted Patents, "[t]he terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right." '423 Patent col.13 ll.22–24. Thus, while a "metal" is necessarily a "conductor," a "conductor" is not necessarily a "metal." Perhaps Claim 23 mistakenly references "contact metal" instead of "conductor." But, at the same time, perhaps Claim 21 mistakenly references "conductor" instead of "contact metal." On the record before the Court, either mistake seems equally plausible. Ultimately, it is not reasonably certain if Claim 23 requires a contact metal regardless of whether the conductor of Claim 21 is metal, or if it requires a conductor that is a metal, or if it requires simply a conductor, or if it has some other meaning.

Accordingly, Defendants have established that the meaning of "contact metal" in Claim 23 of the '261 Patent is not reasonably certain, and the Court finds the term "contact metal" indefinite.

## V. CONCLUSION

The Court adopts the constructions above for the disputed and agreed terms of the Asserted Patents. The Court further finds that Claim 62 of the '423 Patent, Claim 5 of the '395 Patent, and Claim 23 of the '261 Patent are indefinite. Furthermore, the parties should ensure that all testimony that relates to the terms addressed in this Order is constrained by the Court's reasoning. However, in the presence of the jury the parties should not expressly or implicitly refer to each other's claim

construction positions and should not expressly refer to any portion of this Order that is not an actual construction adopted by the Court. The references to the claim construction process should be limited to informing the jury of the constructions adopted by the Court.

**SIGNED this 16th day of October, 2020.**

ROY S. PAYNE
UNITED STATES MAGISTRATE JUDGE